A 5.8 GHz Fully Integrated Low Power Low Phase Noise CMOS LC VCO for WLAN Applications

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Abstract — **A fully integrated low power and low phase noise 5.8 GHz VCO is designed and fabricated in standard 0.24 μm single-poly, 5-metal digital CMOS process. The VCO-core draws 2 mA of current from a 2.5 V supply. Measured phase noise at 1 MHz offset from the center frequency is –112 dBc/Hz. It has a tuning range of 810 MHz with low phase noise performance throughout the tuning range. It meets the requirements for IEEE802.11a WLAN standard. Low power and low phase noise have been achieved simultaneously by the use of np complementary cross-coupled topology. The novel orientation of the inductor pair used in the design minimizes the effect of any unwanted common-mode magnetic coupling that may arise from other on-chip inductors in an integrated environment.**

I. INTRODUCTION

Driven by the exploding growth of the telecommunication market, there is great interest in the development of low power, low cost CMOS solutions for wireless transceiver-front-end. A major challenge lies in the design of fully integrated low power voltage controlled oscillators with low phase noise performance. Considering high frequency and low noise specifications of current wireless LAN standards, LC resonator based oscillators are preferred to relaxation or ring oscillators. Cross-coupled differential LC oscillators have been studied extensively [3-11]. A variant of the cross- coupled LC VCO is the complementary cross-coupled VCO which is chosen for reasons discussed in section III. The VCO, centered around 5.8 GHz, has low phase noise performance and a tuning range of 810 MHz. It meets the requirements for the 5.725-5.825 GHz band of IEEE 802.11a WLAN standard.

The organization of the paper is as follows: section II develops the phase noise requirements for IEEE 802.11a standard, section III discusses the VCO design with justification of the choice of topology; section IV describes design of the planar spiral inductor; section V enumerates varactor design; section VI discusses the VCO with buffers, section VII addresses layout issues, section VIII presents measurement results and section IX concludes the paper.

II. VCO PHASE NOISE REQUIREMENTS

The IEEE 802.11a standard uses Orthogonal Frequency Division Multiplexing (OFDM) based modulation scheme which is more sensitive to phase noise compared to single carrier modulation schemes. Phase noise requirements come from two considerations: (a) interferer strength and (b) sensitivity of OFDM scheme to phase impairments. For the highest data-rate of 54 Mb/s, the standard uses 64-QAM with OFDM in a 20 MHz channel bandwidth [1]. With –65dBm receiver sensitivity and an adjacent interferer 40dB stronger than the desired channel, the VCO phase noise needs to be lower than: $L(17.3\ \text{MHz})$=-40-10log(20 MHz)-19 =-132 dBc/Hz assuming a predetection SNR of 19 dB for a BER of 10^{-6} in 64-QAM system. This translates to a phase noise of –107 dBc/Hz @ 1 MHz offset (considering $1/f^2$ phase noise spectrum). Additionally, phase noise in the OFDM system introduces intercarrier interference (ICI) and leads to a degradation in SNR given as [2]:

$$D_{phase} \approx \frac{11}{6\ln(10)} 4\pi\beta T \frac{E_s}{N_0} \qquad ...(1)$$

where β is the single-sided –3 dB line-width of phase noise power spectral density (assumed to have Lorentzian spectrum), $1/T$ is the subcarrier spacing, E_s is the symbol energy and N_0 is the single sided noise PSD. For SNR degradation less than 0.1 dB, the OFDM link with 64-QAM on a subcarrier spacing of 312.5 KHz and predetection SNR of 19 dB, the –3 dB line width should be at most 31.25 Hz which translates into a phase noise requirement of –110 dBc/Hz @ 1 MHz offset.

So, in order to meet the requirements for IEEE802.11a standard, a VCO should have a phase noise performance of at least –110 dBc/Hz @ 1 MHz offset.

III. CHOICE OF VCO TOPOLOGY

We have analyzed two types of VCO cores: nMOS cross-coupled pair (n-core) and the complementary nMOS-pMOS cross-coupled pair (np-core) with either nMOS or

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pMOS tail current sources (Fig. 1). A comparative study of the topologies may be stated as follows:

(1) *Phase noise perspective:*

For a given power in the current limited region [3], np-core is an improvement over the n-core for two reasons: (a) it has a tank amplitude twice that of the n-core topology for a given current. (b) it can be optimized to have more symmetry in the output waveform leading to further phase noise reduction. However, with increasing tail-current from a low supply voltage the np-core goes into the voltage-limited region rapidly due to reduced voltage headroom. So, if power dissipation is not a concern, the n-core can be driven to give better phase noise performance.

The pMOS tail-current source is better than the nMOS tail-current source because of two reasons: (a) With respect to n-core VCO, the pMOS current source taps the tank-common mode point which has less variation from ac perspective compared to the common-source point tapped by the nMOS source (Fig. 1(a, b)). (b) pMOS has lower flicker noise.

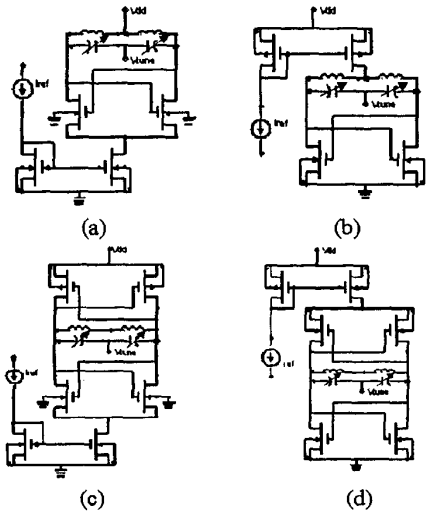

Fig. 1 Differential LC VCOs: n-core with n-/p-tail current source [(a),(b)]; np-core with n-/p-tail current source [(c),(d)]

(2) *Power dissipation perspective*:

The np-core VCO consumes less power for a given phase noise if operated in the current limited region because for the same tail current, output amplitude of the former is twice that of an n-core

(3) *Tuning range perspective*:

The n-core VCO has higher tuning range than np-core topology for equal effective tank transconductance.

Considering the above issues, complementary np cross-coupled core with an nMOS current source is chosen. We have chosen the nMOS current source because, though the pMOS source has marginally better phase noise performance, an np-core VCO with pMOS source goes into voltage limited region for a smaller value of tail current than with an nMOS source.

IV. Inductor Design

The choice of inductance value plays a critical role in phase noise performance of an LC VCO. For better phase noise performance, a smaller inductance value is preferred [4] so long as it satisfies the start-up constraint. Based on this observation, an inductance value of 1.5nH (0.75 nHx2) is chosen for our design. An optimal planar spiral structure for targeted inductance of 0.75nH is obtained using ASITIC simulation tool [12]. Metal-5 and metal-4 are shunted to reduce series resistance. Fig. 2 shows the net *measured* differential quality factor (Q) of the inductor-pair across the tank. Since the one-port quality factor is higher looking from the outer terminal, outer ends are connected to the oscillation nodes.

The inductor pair has been laid out (Fig. 2) such that it achieves (a) positive mutual coupling from a differential perspective (that boosts Q) and (b) minimizes the effect of any unwanted common-mode magnetic coupling that may arise from other on-chip inductors in an integrated environment.

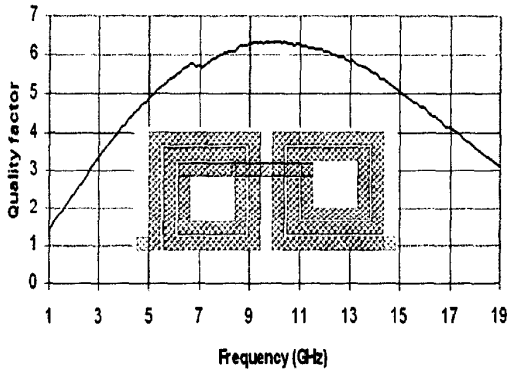

Fig. 2 Measured differential Q of the inductor pair

V. Varactor Design

We have used MOS accumulation varactors with n+ contacts in n-well which offers monotonic capacitance-vs.-voltage profile and does not require any additional mask. The accumulation mode varactor has higher capacitance per unit area and higher quality factor and tuning range compared to reverse-biased pn junction and MOS depletion/inversion varactors. The basic trade-off is between tuning range and quality factor. Shorter gate length improves quality factor by reducing n-well series resistance but decreases the tuning range by increasing the

ratio of fixed overlap capacitance to the variable capacitance. The varactor has a quality factor of more than 15 with a *measured* tuning ratio ($C_{v,max}/C_{v,min}$) of 3.2. No p-type or n-type low drain diffusion implant is present. The variable capacitance can be approximately modeled as hyperbolic-tangent or higher order polynomial function of gate to source/drain voltage. $C_{v,max}$ to $C_{v,min}$ variation occurs through both positive as well as negative values of gate to source/drain voltage. The common mode voltage of the oscillation nodes is chosen such that maximum tuning is obtained when varactor control voltage is varied from 0 to V_{dd}. Gate terminals of the varactors are connected to the oscillation nodes so that the n-well to substrate capacitance appears as common-mode and does not load the tank.

VI. The VCO With Buffers

The switching devices of the VCO core are optimized based on the design trade-offs discussed in section III. The tail current source (600μm/10μm) as well as the mirror (120μm/10μm) has been kept large with moderate W/L so that flicker-noise upconversion is minimized without degrading thermal noise. The transconductances of the nMOS (16μm/0.24μm) and pMOS (50μm/0.24μm) switching devices have been set approximately equal to obtain symmetry in output waveforms [3]. pMOS buffers have been used with inductive peaking to minimize the higher harmonic content of the output waveforms from single-ended perspective.

VII. Layout Issues

Special care is taken to ensure layout symmetry to minimize the even-order distortion in the differential output waveform. The active devices have been laid out with shared source/drains to minimize parasitic capacitance. Differential pairs have a common centroid to minimize the effect of process gradient. The two varactors have been laid out with shared source/drains to minimize the fixed parasitic capacitance. Both active devices and varactors have dummies on either side to improve matching. The gates are connected on both sides to minimize access poly resistance. Substrate taps are provided (in a broken ring fashion) around inductors to reduce substrate noise coupling. The VCO die-photograph is shown in Fig. 3.

VIII. Measurement Results

Fig. 4 shows the time domain waveform of the VCO output as seen in Agilent 83100A oscilloscope. The buffer output (differential) is 0.9 dBm in a 50 ohm system (accounting for 2.8 dB cable loss). Total power consumption is 12.5 mW (VCO core draws 5 mW and output buffers 7.5 mW). Phase noise performance of the VCO has been measured using HP 8563E spectrum analyzer with phase noise measurement utility. Fig. 5 shows the spectrum of the VCO for a center frequency of 5.8 GHz. Phase noise @1 MHz offset from the carrier is –112 dBc/Hz that meets the WLAN requirements with 2 dB margin. Phase noise variation at a particular frequency offset is within 1 dB throughout the tuning range. The measured tuning characteristic of the VCO is shown in Fig. 6. A tuning range of 810 MHz (5.43-6.24 GHz) is measured for control voltage variation from 0 to 2.5V.

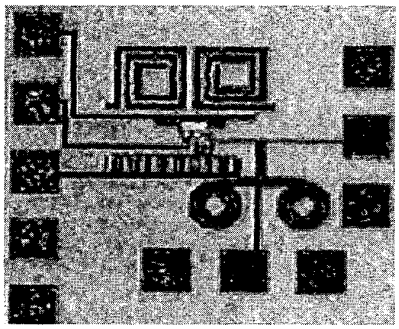

Fig. 3 Die-photograph of the VCO

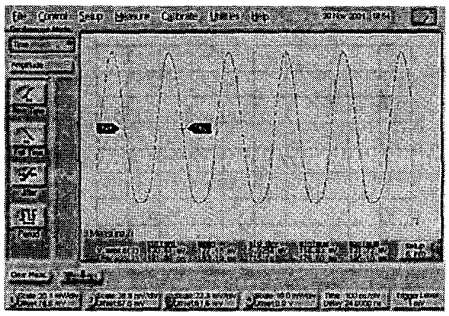

Fig. 4 VCO output waveform (single-ended) as seen in Agilent 86100A oscilloscope

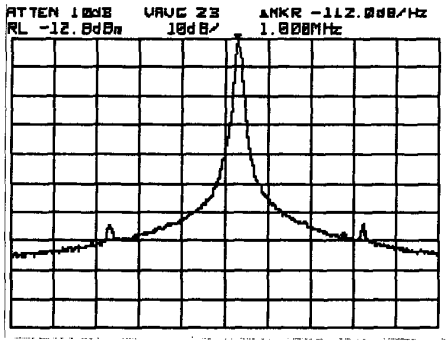

Fig. 5 Spectrum of the VCO at 5.8 GHz observed in HP 8563E

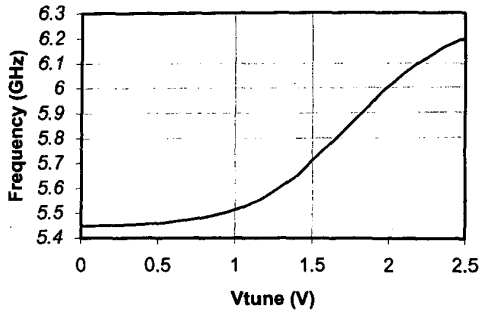

Fig. 6 Measured tuning characteristic of the VCO

Table I compares the measurement results with recently reported fully integrated LC VCOs in standard digital CMOS process, with respect to power dissipation, center frequency and phase noise. The figure of merit (FOM) for phase noise is defined as [4]:

$$FOM = 10\log\left[\frac{kT}{P_{\sup}}\left(\frac{f_0}{f_{off}}\right)^2\right] - S_\phi(f_{off}) \qquad ...(2)$$

where P_{sup} is the power consumed by the VCO, f_0 is the center frequency, f_{off} is the frequency offset from the center, and $S_\phi(f_{off})$ is the phase noise at a frequency f_{off} from the center. This work achieves a good phase noise performance with very low power consumption.

TABLE I
VCO PERFORMANCE COMPARISON

Reference	Center Freq (GHz)	Power Consumed (mW)	FOM for phase noise
[3]	1.8	6	8.7
[4]	2.6	10	3.74
[5]	1.8	6	3.76
[6]	4.7	10.8	-0.89
[7]	5.2	12.5	-20.13
[8]	1.8	32	7.44
[9]	5.35	7	9.12
[10]	2.2	9.13	-0.28
[11]	5	13.8	2.6
This Work	*5.8*	*5*	*6.27*

IX. CONCLUSION

A low power low phase noise fully integrated CMOS differential LC VCO has been presented. Phase noise requirement for the IEEE 802.11a Wireless LAN standard is developed. The VCO core consumes only 5 mW of power from a 2.5 V supply and exceeds the WLAN phase noise requirement over the entire band with at least 2 dB margin. The novel orientation of the inductor structure minimizes the effect of any unwanted common-mode magnetic coupling that may come from other on-chip inductors in an integrated environment.

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